

In re Patent Application of  
**MORIN ET AL.**  
Serial No. Not Yet Assigned  
Filed: Herewith

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In the Claims:

Claims 1-11 (Cancelled).

12. (New) A semiconductor device comprising:  
a semiconductor substrate;  
at least one first MOS transistor and at least one  
second MOS transistor in said semiconductor substrate;  
a dielectric layer on said at least one first MOS  
transistor and on said at least one second MOS transistor;  
a first layer covering said at least one first MOS  
transistor and having a first residual stress level; and  
a second layer covering said at least  
one first MOS transistor and said at least one second MOS  
transistor and having a second residual stress level different  
than the first residual stress level.

13. (New) A semiconductor device according to Claim  
12, wherein said first and second layers have different  
thicknesses.

14. (New) A semiconductor device according to Claim  
12, wherein said dielectric layer includes contact openings  
therethrough for providing electrical connection to said at  
least one first MOS transistor and to said at least one second  
MOS transistor.

15. (New) A semiconductor device according to Claim  
12, wherein said at least one first MOS transistor comprises  
NMOS transistors and said at least one second MOS transistor  
comprises PMOS transistors, and wherein said first and second  
layers have opposite residual stress levels.

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16. (New) A semiconductor device according to Claim 15, wherein said first layer has a positive residual stress level above said NMOS transistors, and said second layer has a negative residual stress level above said PMOS transistors.

17. (New) A semiconductor device according to Claim 12, wherein said at least one first MOS transistor comprises PMOS transistors and said at least one second MOS transistor comprises NMOS transistors, and wherein said first and second layers have opposite residual stress levels.

18. (New) A semiconductor device according to Claim 17, wherein said first layer has a negative residual stress level above said PMOS transistors, and said second layer has a positive residual stress level above said NMOS transistors.

19. (New) A semiconductor device according to Claim 12, wherein a zone formed by said second layer overlapping said first layer has a substantially zero residual stress level.

20. (New) A semiconductor device comprising:  
a semiconductor substrate;  
at least one NMOS transistor and at least one PMOS transistor in said semiconductor substrate;  
a dielectric layer on said at least one NMOS transistor and on said at least one PMOS transistor;  
a first layer covering said at least one NMOS transistor and having a first residual stress level; and  
a second layer covering said at least one NMOS

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transistor and said at least one PMOS transistor and having a second residual stress level different than the first residual stress level.

21. (New) A semiconductor device according to Claim 20, wherein said first and second layers having different thicknesses.

22. (New) A semiconductor device according to Claim 20, wherein said dielectric layer includes contact openings therethrough for providing electrical connection to said at least one NMOS transistor and to said at least one PMOS transistor.

23. (New) A semiconductor device according to Claim 20, wherein said first and second layers have opposite residual stress levels.

24. (New) A semiconductor device according to Claim 23, wherein said first layer has a positive residual stress level above said at least one NMOS transistor, and said second layer has a negative residual stress level above said at least one PMOS transistor.

25. (New) A semiconductor device according to Claim 20, wherein a zone formed by said second layer overlapping said first layer has a substantially zero residual stress level.

26. (New) A semiconductor device comprising:  
a semiconductor substrate;

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at least one PMOS transistor and at least one NMOS transistor in said semiconductor substrate;

a dielectric layer on said at least one PMOS transistor and on said at least one NMOS transistors;

a first layer covering said at least one PMOS transistor and having a first residual stress level; and

a second layer covering said at least one PMOS transistor and said at least one NMOS transistor and having a second residual stress level different than the first residual stress level.

27. (New) A semiconductor device according to Claim 26, wherein said first and second layers have different thicknesses.

28. (New) A semiconductor device according to Claim 26, wherein said dielectric layer includes contact openings therethrough for providing electrical connection to said at least one PMOS transistor and to said at least one NMOS transistor.

29. (New) A semiconductor device according to Claim 26, wherein said first and second layers have opposite residual stress levels.

30. (New) A semiconductor device according to Claim 29, wherein said first layer has a negative residual stress level above said at least one PMOS transistor, and said second layer has a positive residual stress level above said at least one NMOS transistor.

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31. (New) A semiconductor device according to Claim 26, wherein a zone formed by said second layer overlapping said first layer has a substantially zero residual stress level.

32. (New) A method for fabricating a semiconductor device comprising:

forming at least one first MOS transistor and at least one second MOS transistor in a semiconductor substrate;  
forming a dielectric layer on the at least one first MOS transistor and on the at least one second MOS transistor;  
forming a first layer covering the at least one first MOS transistor and having a first residual stress level;  
and

forming a second layer covering the at least one first MOS transistor and the at least one second MOS transistor and having a second residual stress level different than the first residual stress level.

33. (New) A method according to Claim 32, wherein the first and second layers have different thicknesses.

34. (New) A method according to Claim 32, further comprising forming contact openings through the dielectric layer for providing electrical connection to the at least one first MOS transistor and to the at least one second MOS transistor.

35. (New) A method according to Claim 32, wherein forming the first layer comprises:

forming the first layer covering the at least one

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first MOS transistor and the at least one second MOS  
transistor;

forming a mask on the at least one first MOS  
transistor;

removing the first layer on the at least one second  
MOS transistor; and

removing the mask.

36. (New) A method according to Claim 32, further  
comprising performing a localized treatment of the first and  
second layers that overlap the at least one first MOS  
transistor for modifying the second residual stress level of  
the second layer.

37. (New) A method according to Claim 36, wherein  
performing the localized treatment comprises implanting ions  
into the second layer.

38. (New) A method according to Claim 37, wherein  
germanium ions are implanted into the second layer.